

## VHDL

### Traffic Light Controller

#### Assignment Overview

This assignment has been set to get you familiar with Algorithmic State Machines (ASM) for designing sequential logic circuits and synthesising them from a VHDL description. You should develop your design using Altera's Quartus II V6.0 and test your design on the NIOS board. You **MUST** test your design on the Altera boards and include a signed Demonstrator sheet with your report.

#### Assignment Outline

The objective of this assignment is to design and implement a circuit for controlling traffic lights at the junction of two main roads. Both roads have car sensors for detecting cars on the road. If there are cars on both roads then changing the light of the traffic lights is as follows.

SN green, EW red for long-timeout , then

SN yellow, EW red for short-timeout, then

SN red, EW red for short-timeout second, then

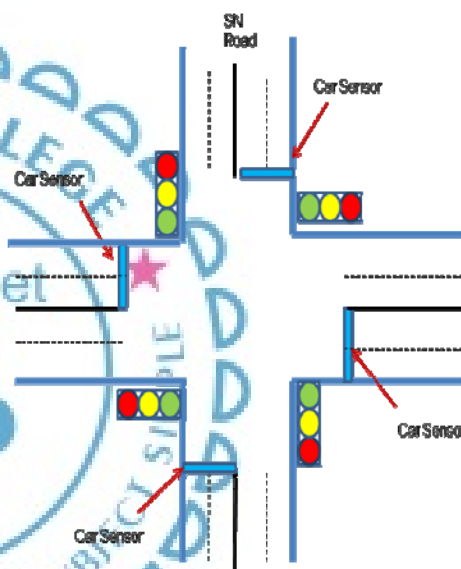
SN red, EW green for a long-timeout, then

SN red, EW yellow for short-timeout, then

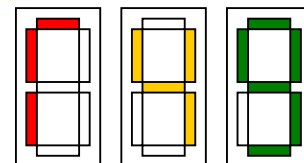
SN red, EW red for short-timeout, then

SN green, EW red for long-timeout .....

If there is no car on one road then its lights will remain red after finishing its red light period and the other road's light will remain green.



The car sensors will be the push-buttons on the board. Display **g**, **y**, and **r** letters on the board's two seven segments to represent the traffic lights.



You will need to design a debouncing block to debounce the inputs from the push-buttons, one or two timers for generating the short and long timeouts, and the controller.

Use your first and second names or their abbreviations for naming the car sensors and traffic lights. The short and long timeouts for each student are according to the attached table.

Create a symbol for each module of your design and interconnect them in the top level block diagram file.

## Reports

Your report should include the following.

1. Description of the architecture of your design with block diagram showing interconnections.
2. Description of each module to be documented by the following information:
  - a. **Commented** VHDL code for each module.
  - b. Full simulation of each module. (With **annotations** indicating what the simulation proves).
3. Schematic of the full system.
4. Simulation of the full system. (With annotations and maximum ½ page on any comments)
5. Explanation of experimental test results.
6. Conclusion (Maximum ½ page)
7. Demonstrators check sheet
8. You should also submit your design via VITAL. Make sure all the files need to compile, simulate, and test the design are included.

## Warning

When marking the reports I will be looking very closely for any signs of collusion, as this is unacceptable. If I find any evidence of collusion then all students will receive 0. The points that I will be looking for, to indicate collusion, will be similar filenames, similar variable names, similar test waveforms etc. If you do collude I will spot it and you will be penalised – you have been warned.

