

Find the parasitic delay and logical effort of the X2 and X4 NOR gate A input. By what percentage do they differ from that of the X1 gate?

An output pad contains a chain of successively larger inverters to drive the (relatively) enormous off-chip capacitance. If the first inverter in the chain has an input capacitance of 20fF and the off-chip load is 10pF, how many inverters should be used to drive the load with least delay? Estimate this delay, expressed in FO4 inverter delays.